The Bleeding Edge – Part III:

Emerging Applications in Nanoelectronics

Today, completing set of three lectures: Use of nano for information technology

Including:

1) The REAL size of transistors and their shrinkage

2) Why they can't get much smaller (including the POWER PROBLEM)

3) Weird NEW switches that might circumvent power and scaling problems:

QCA, Single electron transistors / NDR . . .

= Routes toward a true successor nanoelectonic technology?

Echoing the first lecture: What IS nanoelectronics?

Microelectronics HAS shrunk to near nanometer size

But does that imply "nanoelectronics" is just a new name for microelectronics?

In other words, that it qualifies as "nano" based only on a technicality

Or, following my first lecture definition, might it be fundamentally different?

Where smallness makes things act in unprecedented and unexpected ways

To answer, we need to look more closely at the shrinkage of microelectronics

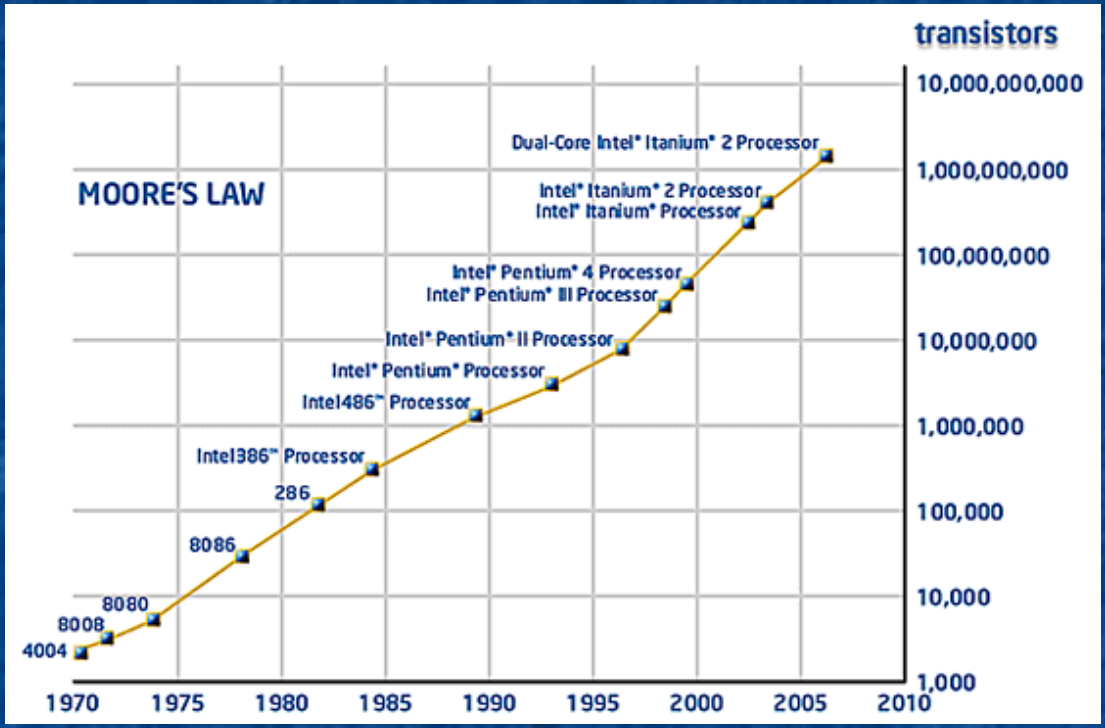
Bringing us back to "Moore's Law:"

Moore's Law revisited:

Which is not really a law, but an after dinner speech that went viral!

Intel's (self-inflicted) curse:

(Because Wall Street now **expects** it to be followed)



"Integrated circuit complexity (# of transistors) doubles ~ every 18-24 months"

What has driven this increase in complexity?

Possibility #1: Circuits have gotten larger (more area => fit in more transistors)

No!: Original 1960's IC's were about 1 cm^2 in area

Modern microprocessors might reach 10 cm^2 (net growth of only 10X)

Possibility #2: Individual transistors have gotten MUCH smaller

Yes! = "Nodes" – numbers that sort of describe transistor's size:

Year	1971	1982	1989	1994	2004	2008	2012	2014
Node	10 um	1.5 um	800 nm	600 nm	90nm	45 nm	22 nm	14 nm

That seems like a strange sequence of numbers?

It originally denoted wavelength of UV light source used in making the circuit
=> smallest ("diffraction limited") circuit feature

But that means, at least by one definition, IC's ARE nano!

Yes and no:

First, they were already embellishing things a bit:

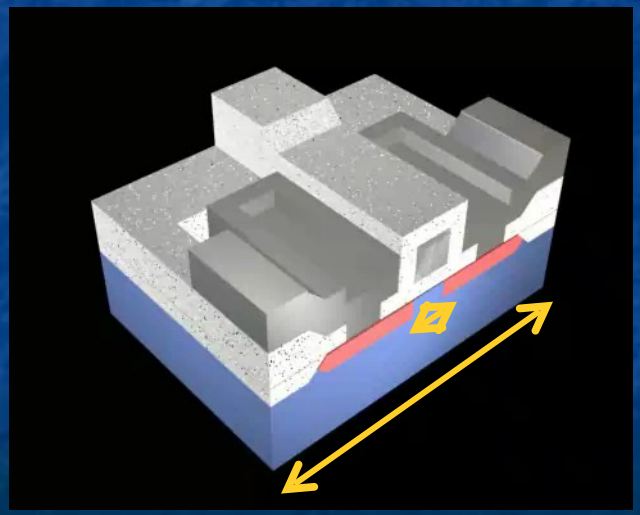
Nodes = "smallest feature size"

E.g. the width of a metal line, or size of an oxide mesa

Transistors have many such features, hence they are 5-10 times larger

"Feature" (gate electrode)

vs. full transistor size:



https://WeCanFigureThisOut.org/VL/IC_process.htm

And then it gets even fuzzier

"The End of the Shrink" - IEEE* Spectrum magazine (November 2013)

*IEEE = Institute of Electrical & Electronic Engineers (international, almost half million members)

"The relationship between node names and chip dimensions is far from straightforward. Nowadays, a particular node name does not reflect the size of any particular chip feature"

The reporter asked:

"What do you mean by 14 nm?'"

She (a vice president for process development at IMEC):

"let out a wry, knowing laugh . . .'Ah ... what's in a name? Actually not that much any more.'"

So no, even leading edge IC's are not truly "nanoelectronics"

They are instead being held back by several factors:

1) "Diffraction limited focusing" => Can't make beams narrower than wavelength

Well, just continue moving to even smaller wavelengths, right?

Go much smaller and UV light becomes X-ray "light"

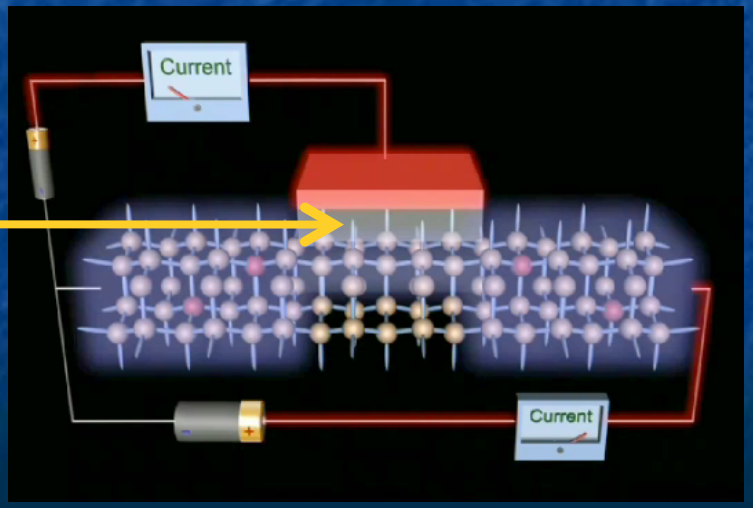
Which doesn't slow down much in materials => Can't make lenses!!

2) "Electron tunneling" => Electrons tunnel THROUGH insulators < 1 nm thick

But MOSFET transistors DEPEND

on insulating layer BLOCKING

electron flow from "gate" into body



https://WeCanFigureThisOut.org/VL/MOS_kit.htm

Plus one more HOT problem: Power

Smaller transistors => You can fit in more per area of circuit (=> Moore's Law)

Smaller transistors => Smaller power required to operate each transistor

HOWEVER for MOSFET transistors (the workhorse of the IC industry):

As size shrinks, power consumption does not fall as rapidly

So an IC packed with smaller transistors consumes MORE power / area!

Big deal . . . Buy an extra/bigger battery!

No, there can be more significant ramifications:

Notice how **"notebook"** computers replaced **"laptop"** computers? Know why?

Computers got so **HOT** they can burn your lap - So lawyers said change name!

Evolution of power density in microprocessors

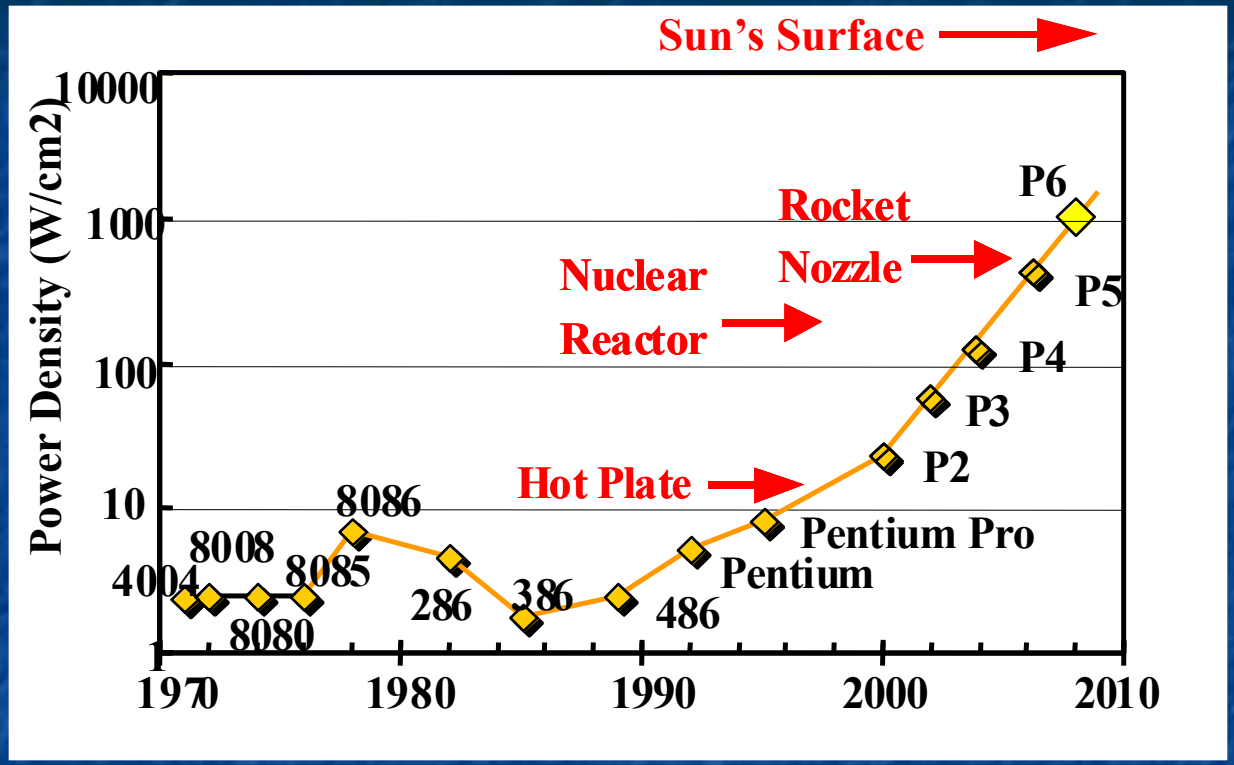


Figure courtesy of Prof. Greg Snider, U. Notre Dame

YES! Power density in modern microprocessor > that put out by rocket nozzle

And is heading (rapidly) for power/area of SUN's SURFACE (!!@#!!)

So there is a big incentive to "get weird"

To develop devices very UNLIKE present day field effect transistors

Devices with far less charge movement => MUCH lower power per device

Maybe even devices that don't move charge:

Based on nano magnetism (a.k.a. atomic "spin")?

Based on photons? (but they are so darned big!)

Based on . . . (?)

Or **devices that are NOT intrinsically analog** (as today's transistors are)

You'd no longer need a surrounding circuit to force digital behavior

Intrinsically digital devices could instead stand alone: One device = 1 bit

Quantum Mechanics to the rescue (because you can't get much weirder)!

Getting weird with Quantum Mechanical Tunneling

Here we need to remember the full details of tunneling (from third lecture):

Tunneling occurs when an electron wave tries to penetrate an energy barrier

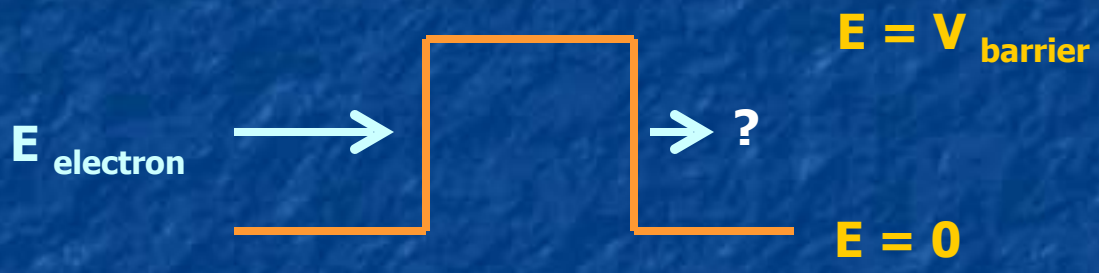
Energy barrier is formed in gaps between conducting materials:

THIS gap is higher energy because it lacks the positive nuclei that electrons like

A "Gap" would also be higher energy if it contained an excess of negative charge

Probability an electron can tunnel through such a barrier?

From the earlier lecture on electron waves, for a gap energy barrier like this:



We learned that, within the barrier, the electron wavefunctions die away as:

$$\Psi(x)^2 = C\, e^{-2kx} \qquad \text{where} \qquad k = \sqrt{[2m(V_{barrier} - E_{electron}) / h_{bar}^2]}$$

Bigger k is, faster the wave dies away! Less left over to continue on other side!!

Key factor in k is V-E = how high barrier towers above electron (in energy)

Giving tunneling probabilities for various kinds of barriers:

Barrier:	0.1 nm	0.3 nm	1 nm	3 nm	10 nm
Similar material (0.2 eV)	0.63	0.25	0.01	1×10^{-6}	$< 10^{-15}$
Insulator (2 eV)	0.36	0.046	3×10^{-5}	4×10^{-14}	$< 10^{-15}$
Air / Vacuum (4 eV)	0.13	2×10^{-3}	1×10^{-9}	$< 10^{-15}$	$< 10^{-15}$

Through vacuum ($\Delta E \sim 4$ eV) can only go fraction of nm:

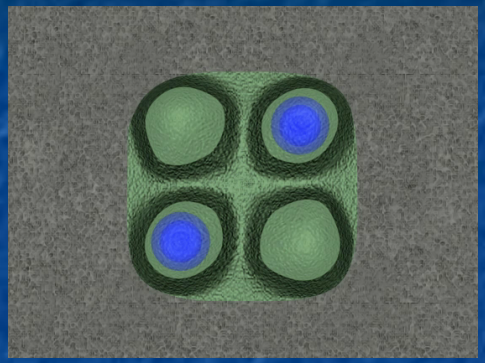
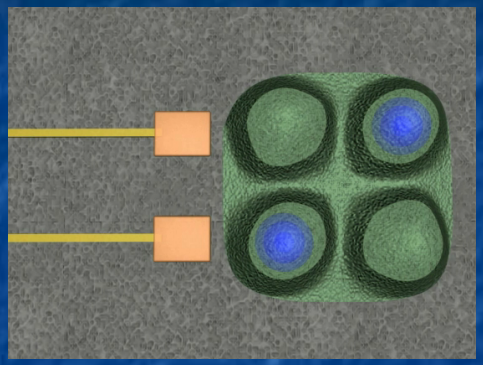
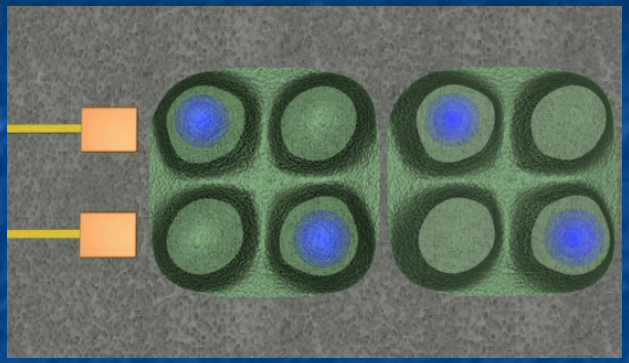
Basis for STMs we use in lab

But through lower barriers, retain finite tunneling probabilities for 1-3 nanometers:

Basis for MANY nanodevices ***Examples?***

As applied to "Quantum Cellular Automata"

Introduced in lecture on self-assembly - But what is their necessary scale?

To switch between logic states, electrons must move between dots

Option 1: Jump through vacuum → ΔE ~ 4 eV Separation needed < tenths of nm

That's atomic spacing! QCA dots would have to be individual atoms!

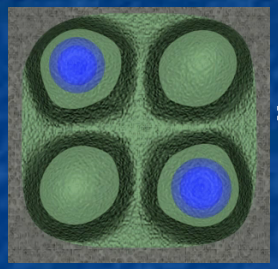
Option 2: Jump through substrate → ΔE ~ 0.2 eV Separation needed < few nm

Dots ~ tens of nanometers (possible, remember self-assembled quantum fortresses?)

ALSO would be about right size if dot is to accommodate only one extra electron

How to make QCA cells into powerful (yet simple) digital devices:

1) Define one electron arrangement as a digital “0” and the other as a digital “1”



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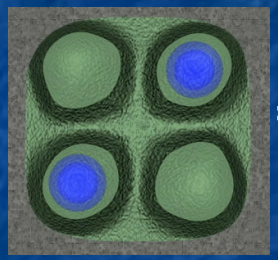

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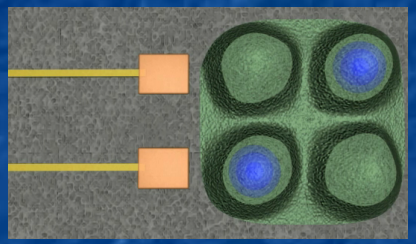
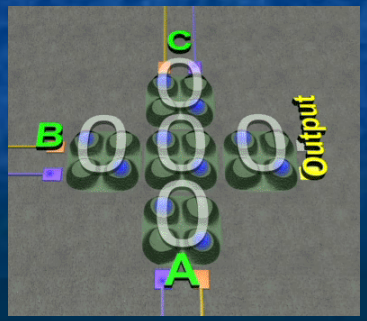
2) Bring in plus and minus charged metal lines to program cell

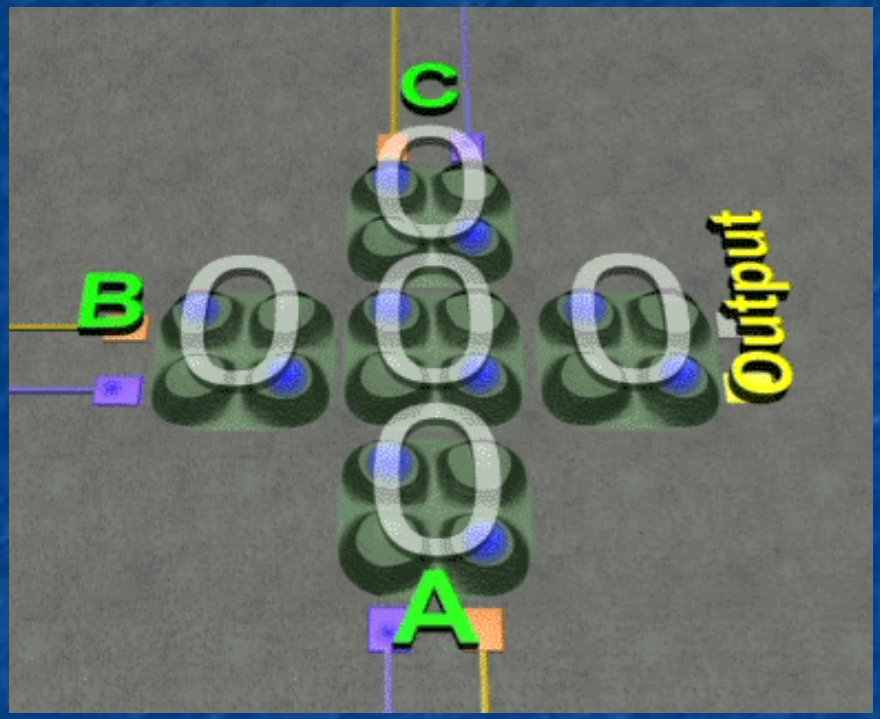


3) Then arrange five cells like this



This functions as a digital MAJORITY gate:

Three input votes (A, B, C) => Majority vote on output:

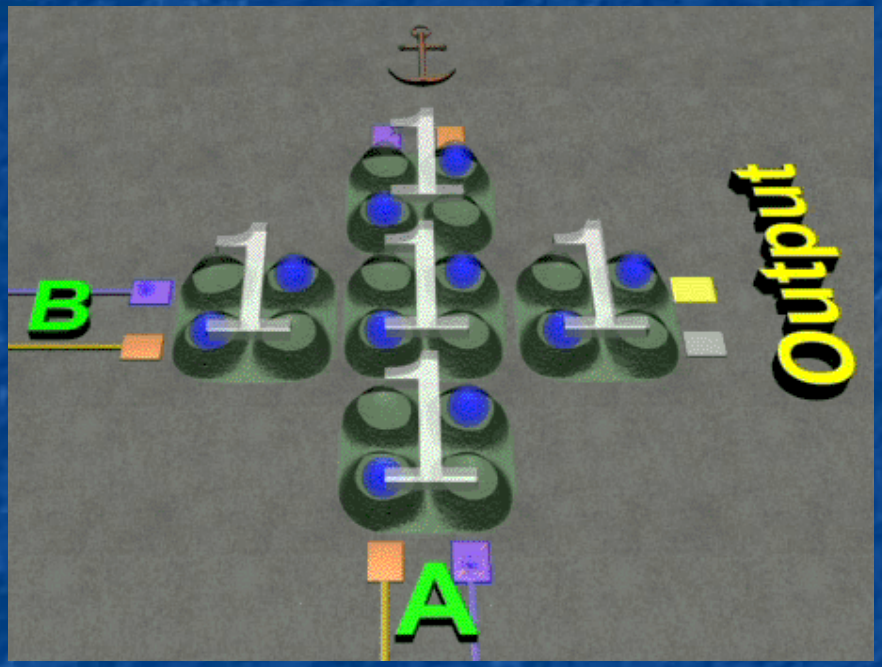


Supporting webpage with animated explanation of QCA MAJORITY gate function:
Bleeding Edge Nanoelectronics - Supporting Materials - QCA MAJORITY

If instead hold one input at 1, functions as a digital OR gate:

Fix top input at 1 (anchor via fixed voltages on its input metal lines - not shown)

Then get 1 out if either A OR B input goes to 1 (guarantees majority of 1's)

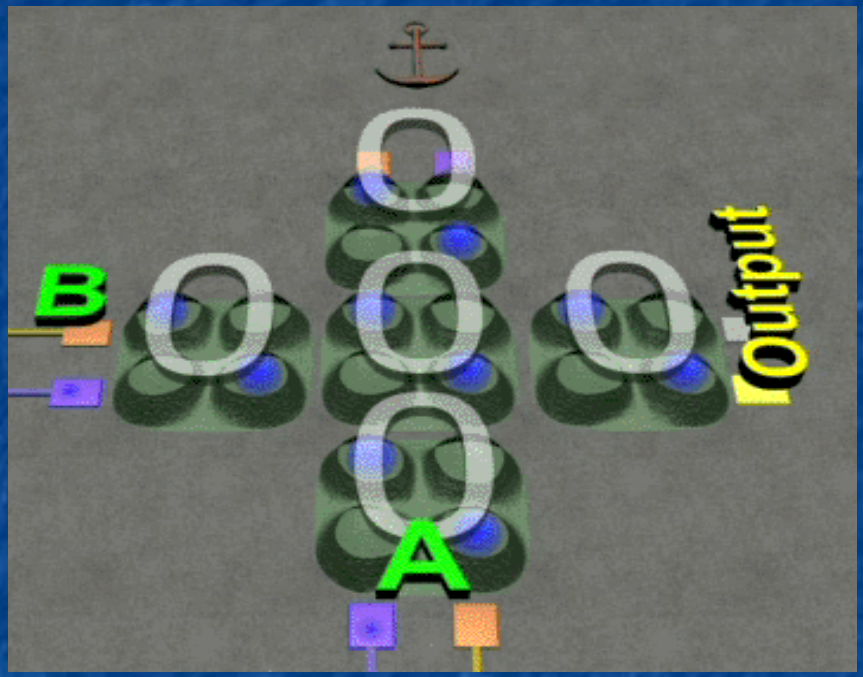


Supporting webpage with animated explanation of QCA OR gate function:
Bleeding Edge Nanoelectronics - Supporting Materials - QCA OR

If hold one input at 0, functions as a digital AND gate:

Fix top input at 0 (anchor via fixed voltages on its input metal lines - not shown)

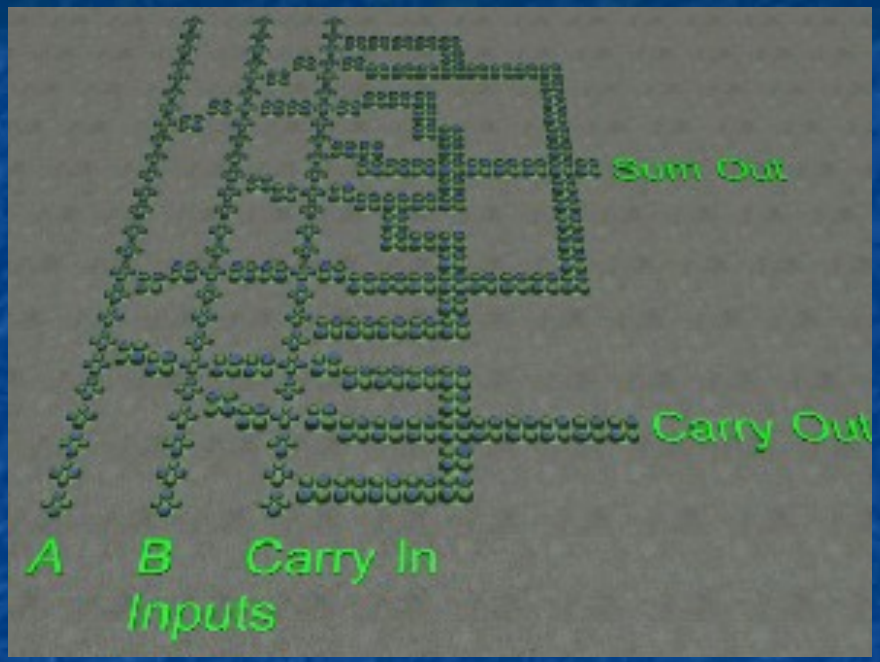
Then to get 1 out, both A AND B must be at 1 (to get majority of 1's)



Supporting webpage with animated explanation of QCA AND gate function:
[Bleeding Edge Nanoelectronics - Supporting Materials - QCA AND]

In addition to Boolean logic, QCA's can do math:

Layout of QCA cells required to add digital inputs => digital sum and carry bit:

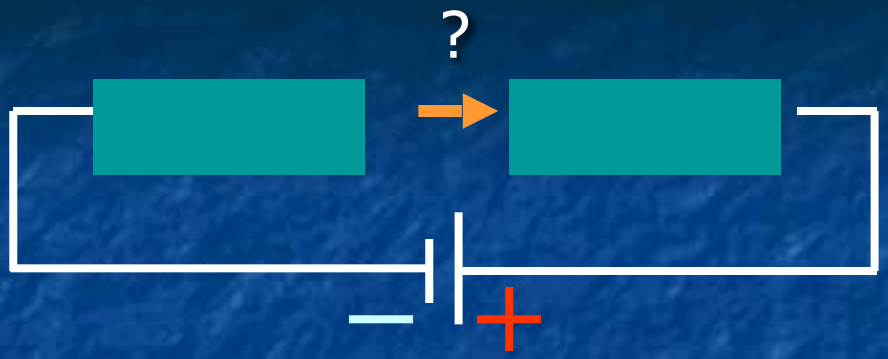


Adder circuit can then be easily modified to subtract => multiplication and division

Together, provide functionality necessary for a quantum dot computer

(DISCLAIMER: QCA still has problems with **direction** of information flow and clocking of data)

Second "weird" idea: Devices using tunneling CURRENT



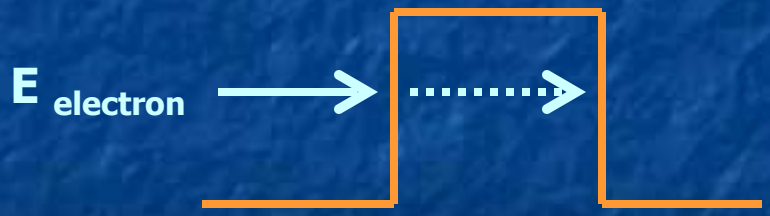
Your intuition probably says the current will increase as you increase the voltage

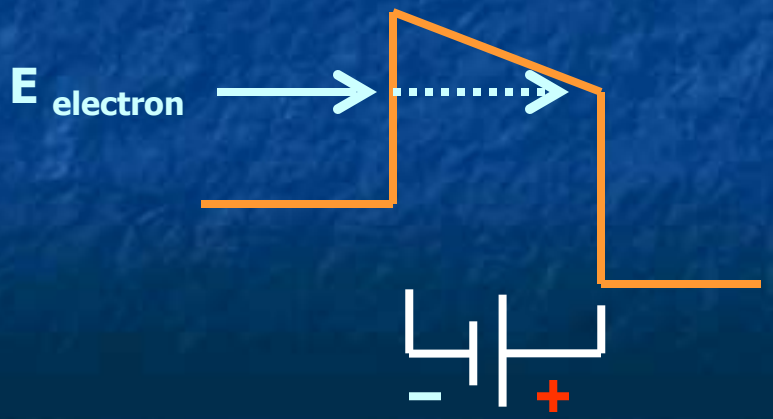
But don't see anything about voltages and electric fields on preceding pages

They enter through their effect on the barrier:

Voltage → *Electric Field*

→ *Energy decrease to right*





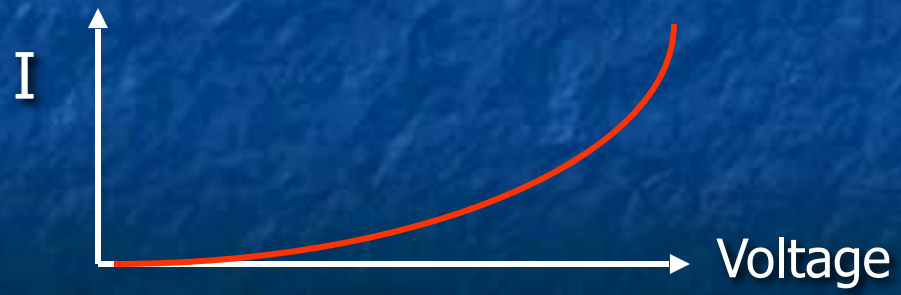
As electron tunnels through barrier, its height decreases

Analogous to series of very thin barriers of decreasing height:

"Barriers" less & less troublesome as move to right → less effective at diminishing current flow

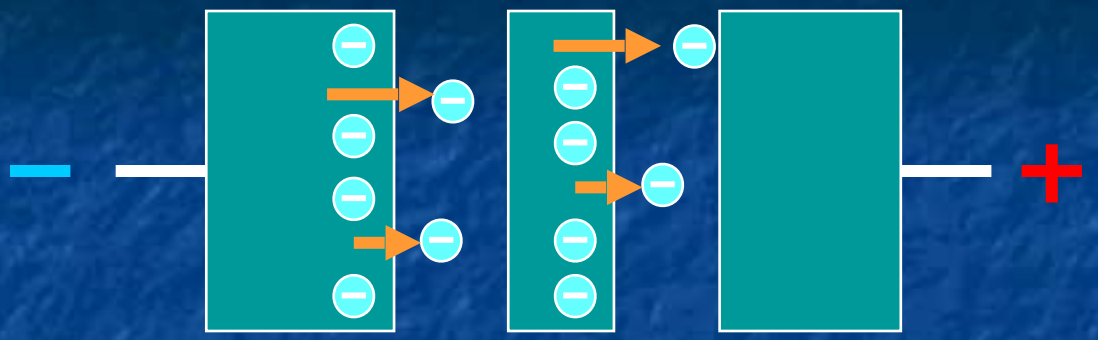
So your intuition IS correct Further, more voltage → more tilt → much weaker net barrier

So expect tunneling current vs. applied voltage to go something like:

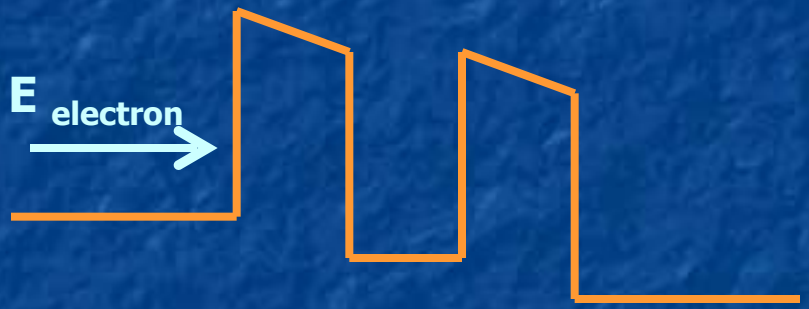


Tunneling current across 2 gaps in series?

Physical Structure:

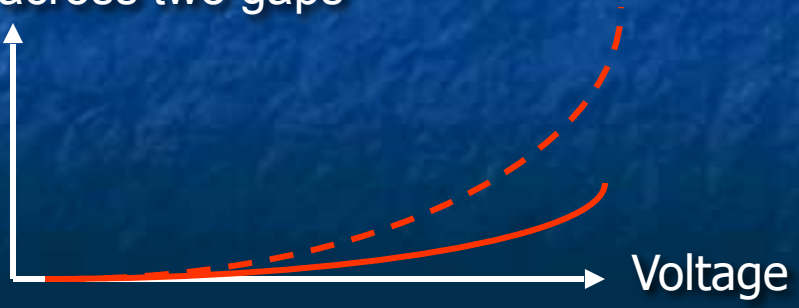


Barrier diagram:



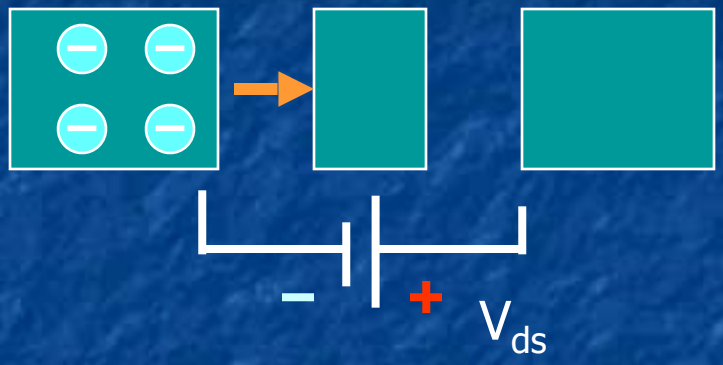
Can still tunnel. But twice as hard to tunnel across two gaps

So likely just get less current:

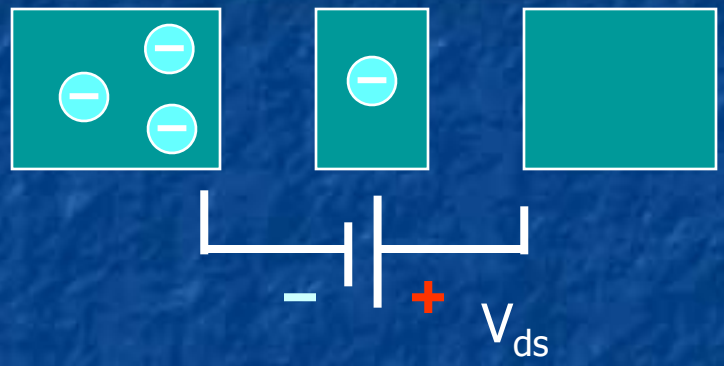


But this all changes when things get really small

Tunneling current starts flowing:



But then runs into a problem:



Charge added to middle "quantum dot" repels charges trying to follow!

There is just not enough room on nano center dot for TWO negative charges to happily coexist

Result is that more charges jump from left ONLY when center charge jumps off to right

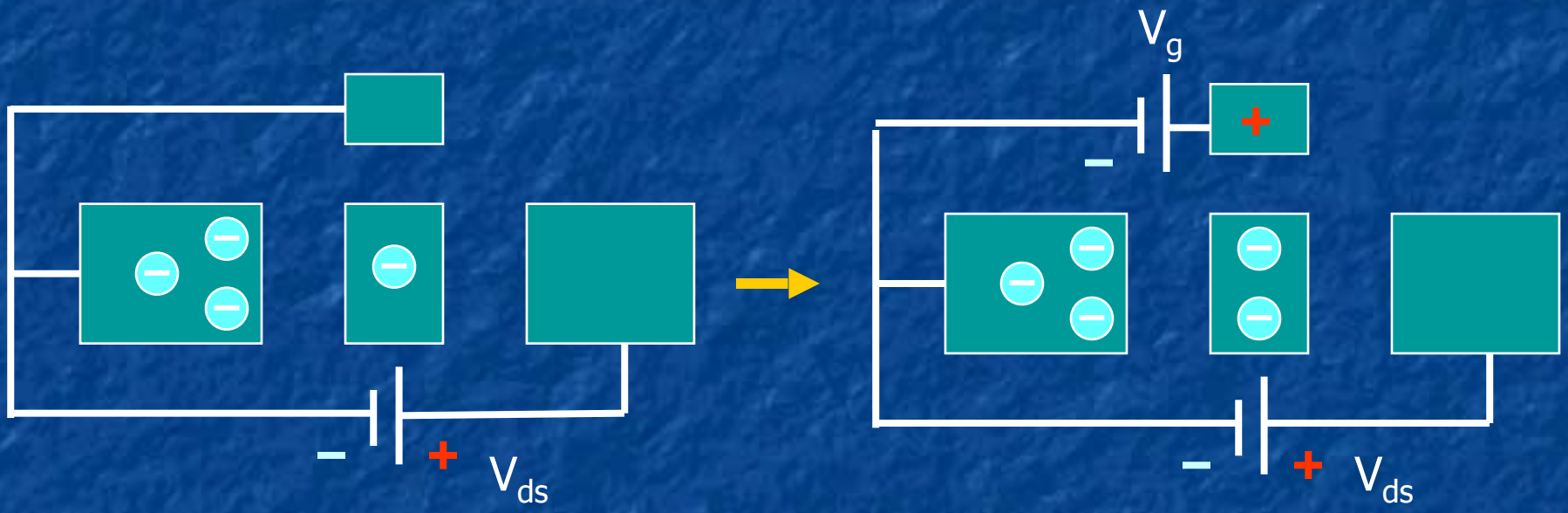
Blockage is caused by charge repulsion in confined space

Charge repulsion also called “coulomb repulsion" so phenomena is known as

COULOMB BLOCKADE

So "Coulomb Blockading" will just further limit current?

Yes, but can counter by adding another electrode to side of center Q-dot

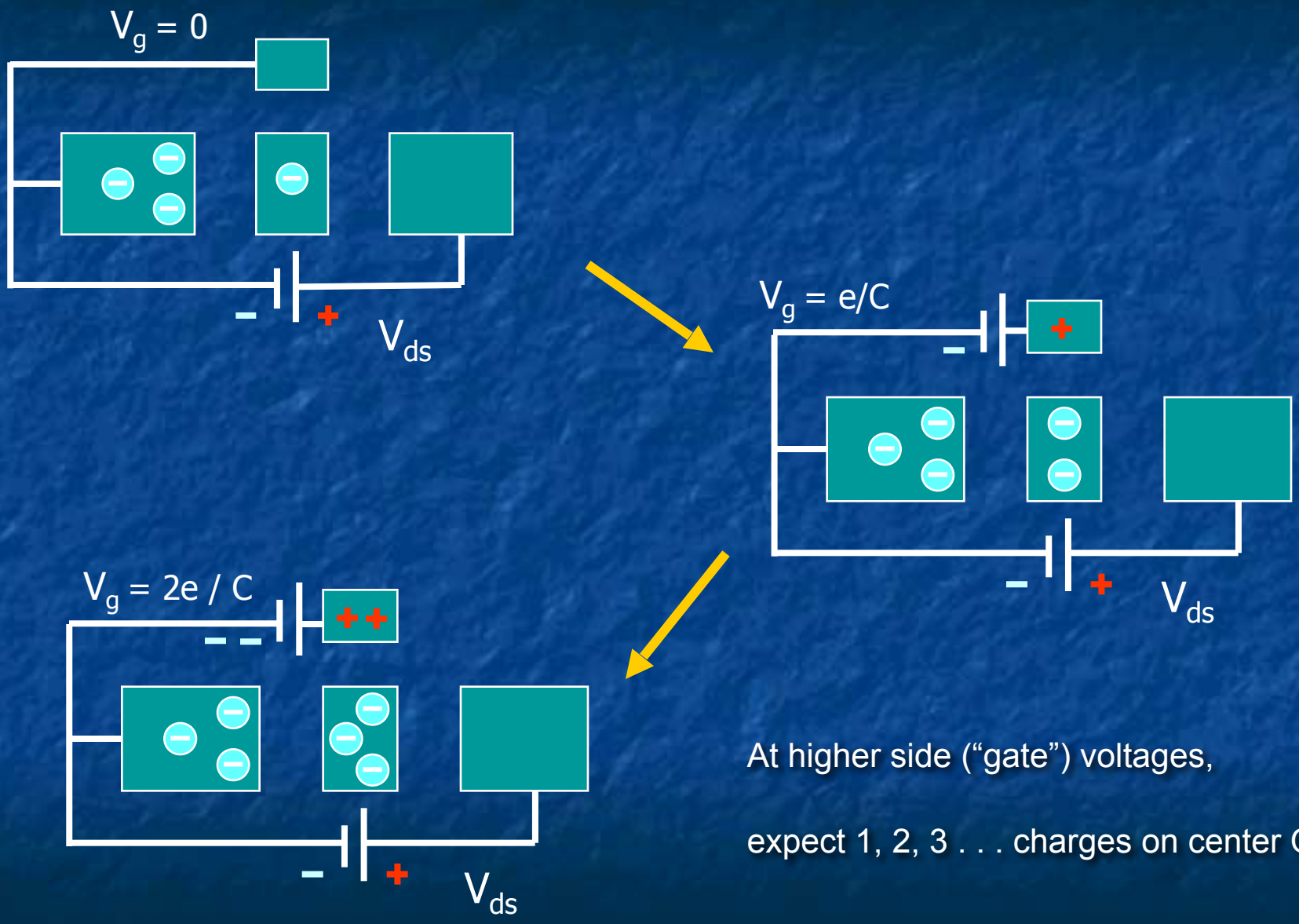


On center Q-dot, repulsion between two electrons had prevented two from jumping on

But now side "gate" counters this by adding nearby attractive positive charge

For the EE's: The side gate electrode is forming a charging capacitor with the Q-dot

And as you further increase attractive voltage on side gate:

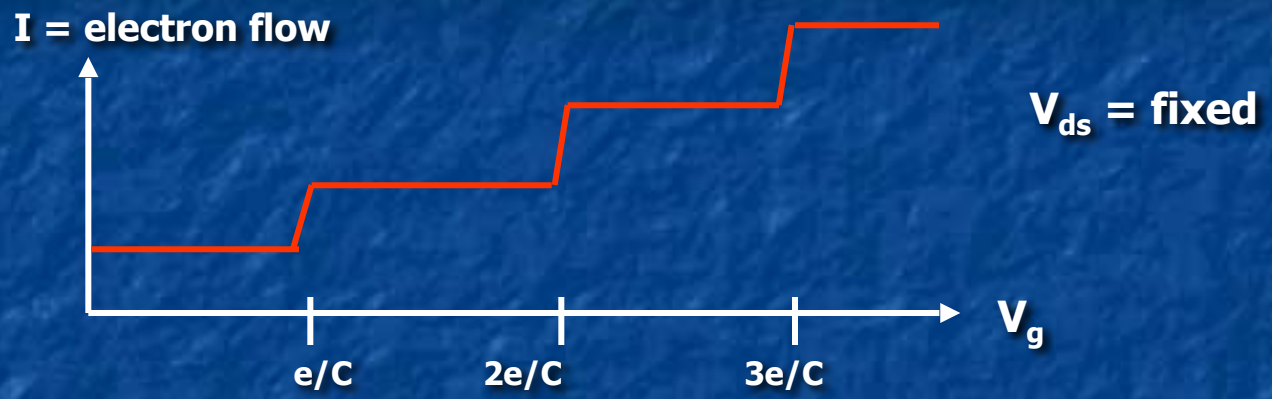


At higher side (“gate”) voltages,

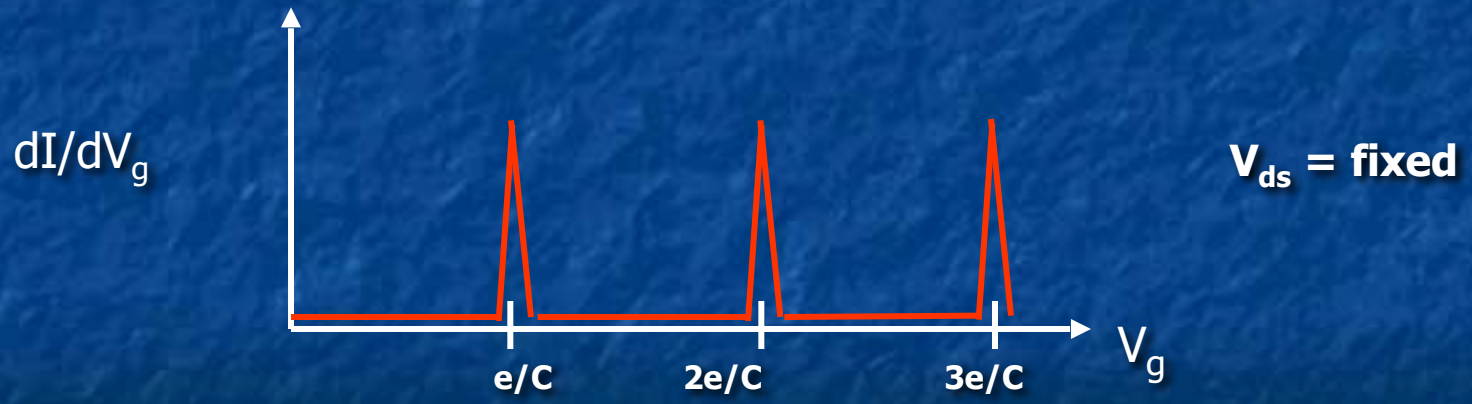
expect 1, 2, 3 . . . charges on center Q-dot

Giving this electrical behavior:

With fixed end-to-end voltage (V_{ds}), as you ramp up side gate voltage (V_g) expect:

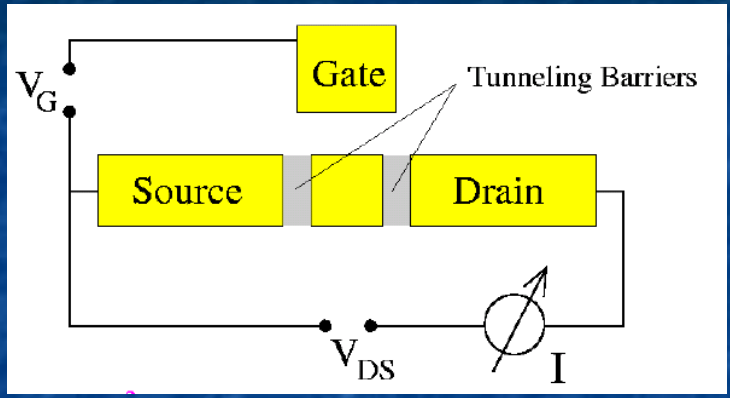


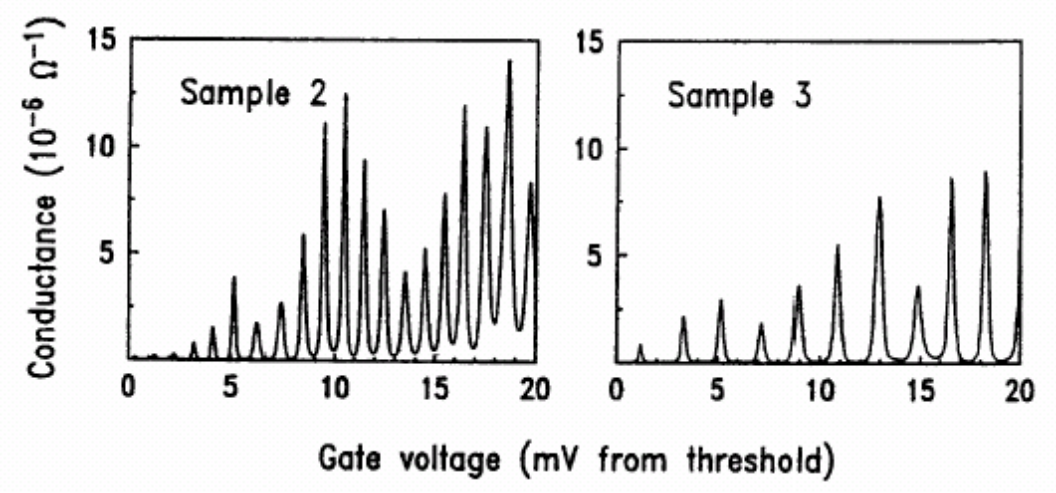
Or plotting the slope (known as the "conductance" = dI/dV_g):



(for explanation of magic voltages above, see appendix at the end of this lecture)

Which is indeed seen in "Single Electron Transistors" (SETs)



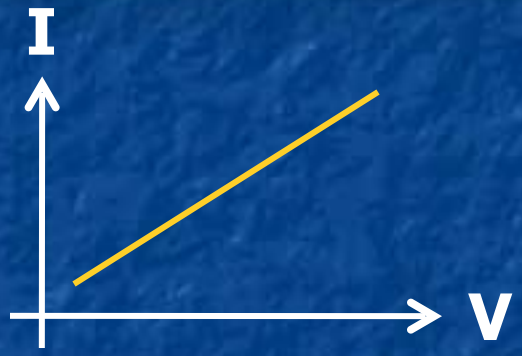


Third weird (but related) idea: Negative Differential Resistance (NDR)

"Resistance" = resistance to electron flow when push (from Voltage) is applied

If electron flow (current = "I")

increased in proportion to push (Voltage):



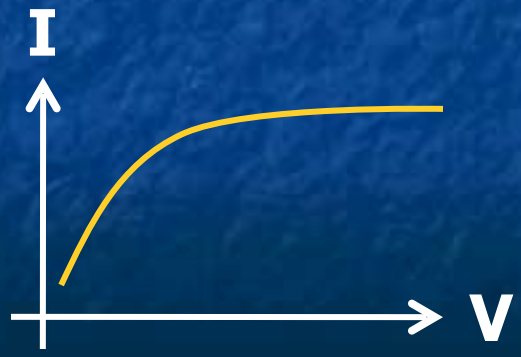
Steeper the slope, more current per push => less "resistance"

So "resistance" = reciprocal of slope = dV/dI (constant in plot above)

But for many things, including transistors, slope is NOT constant:

MOSFET "I-V characteristic:"

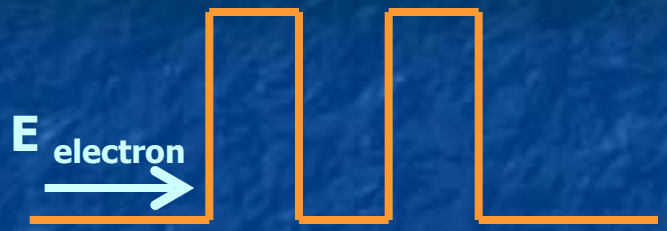
Slope falls, resistance increases as push harder



What if slope actually went negative?

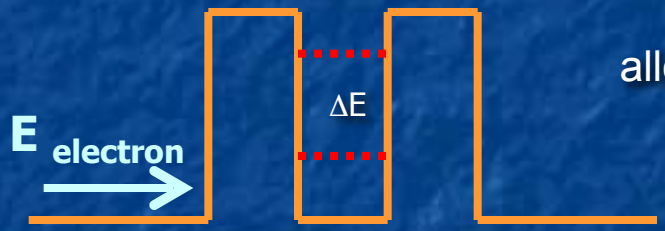
What would happen, and how might I exploit it?

One way to achieve: TWO closely spaced barriers:



BETWEEN the two barriers the electron is in a box => STANDING WAVES

Which can only have certain specific wavelengths and thus specific energies



Electron from left needs to briefly rest on allowed energy level between barriers

Or else it would have to tunnel complete distance in one hop (~ impossible)

So to cross, incoming energy must match up with one of the standing wave levels!

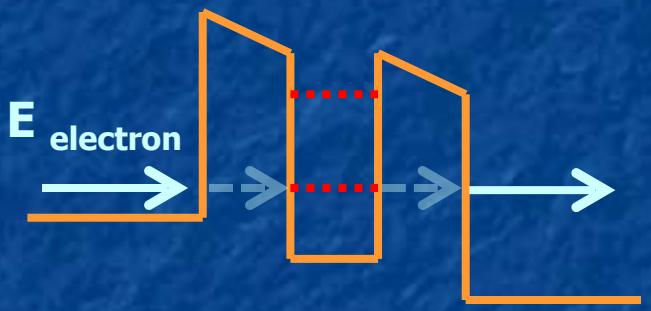
Or, can "tune" positions by applying an end to end voltage:

Assume (realistically) that left, center and right are conductors

Then ~ all of voltage drop occurs across the insulating spacer barriers

(Note: voltage = energy / charge, and electric field = voltage / distance)

Leading to energy vs. position diagram of:

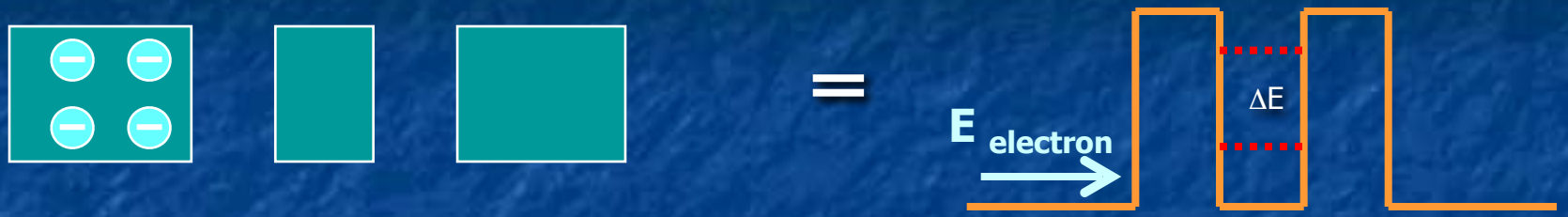


Certain applied voltages will PULL center levels down to match incoming energy

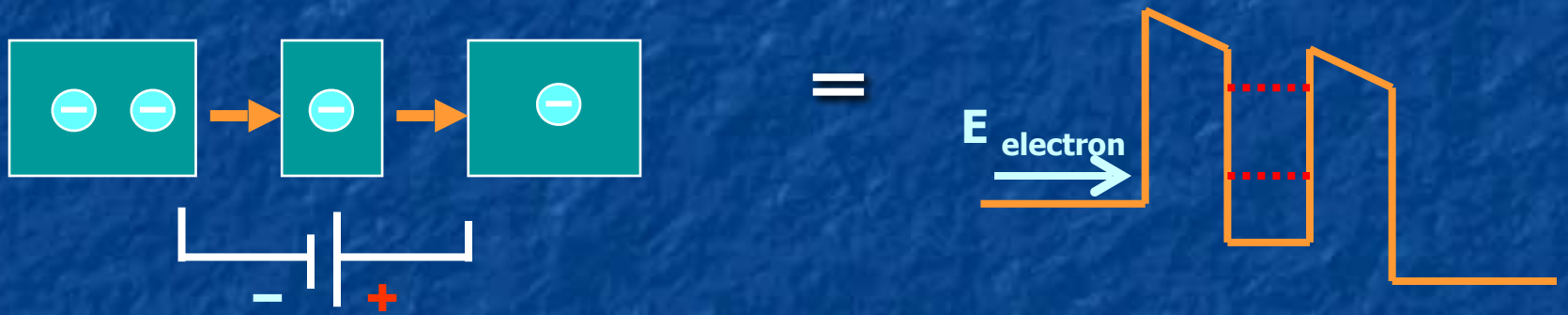
At only(!) those voltages will we get strong current through the nano-device

Actual physical structure would look more like:

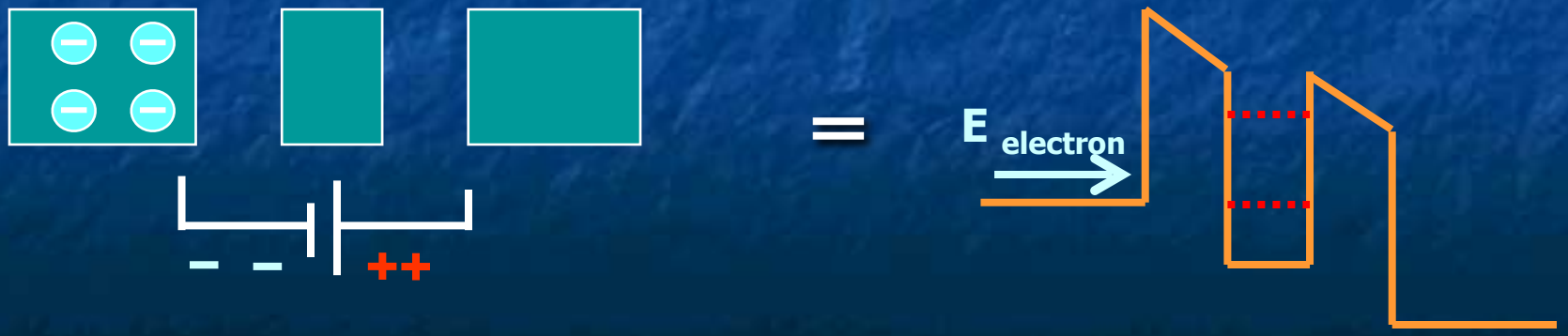
NO voltage applied => No match of levels => little or no electron flow



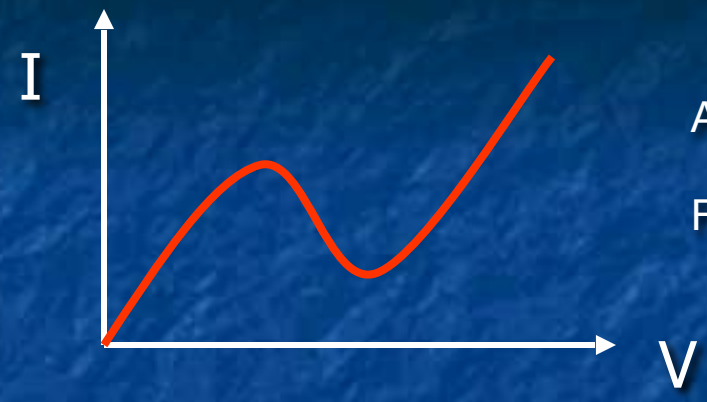
WITH medium voltage applied => MATCH! => current flow



With larger voltage applied => Match is lost => little or no electron flow



But eventually there'd be match with 2nd level, producing:



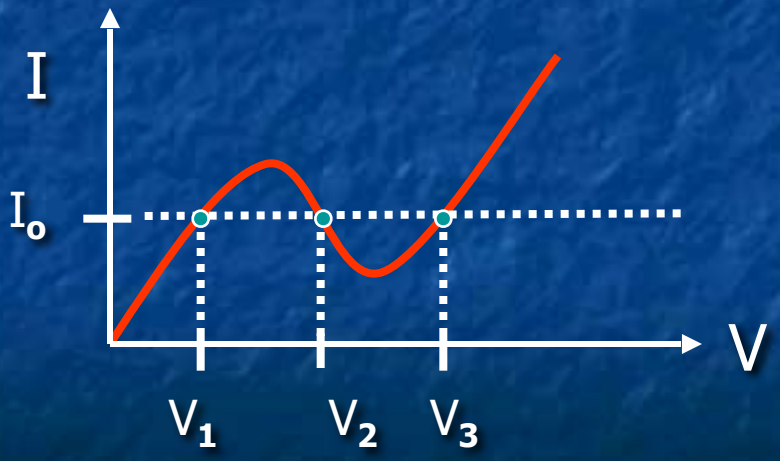
As voltage increases, get one (or more) peaks in current

Followed by valleys

"Negative Differential Resistance" - NDR

(because I vs. V slope is briefly negative)

Useful? What if external circuit only allowed one fixed current through NDR device?



NDR device MUST be at one of three voltages

Can be shown that it won't STAY at V_2

But still left with TWO stable voltages V_1 or V_3

Digital "0" and digital "1"

Hold it!

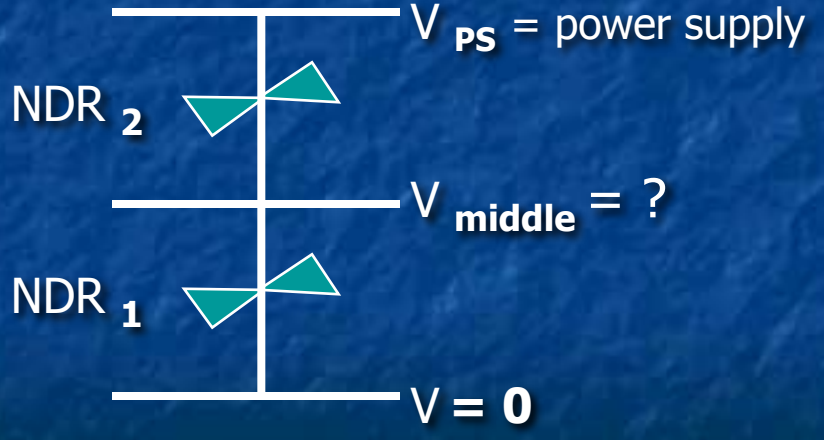
Doesn't attached constant current circuit = added complexity elsewhere?

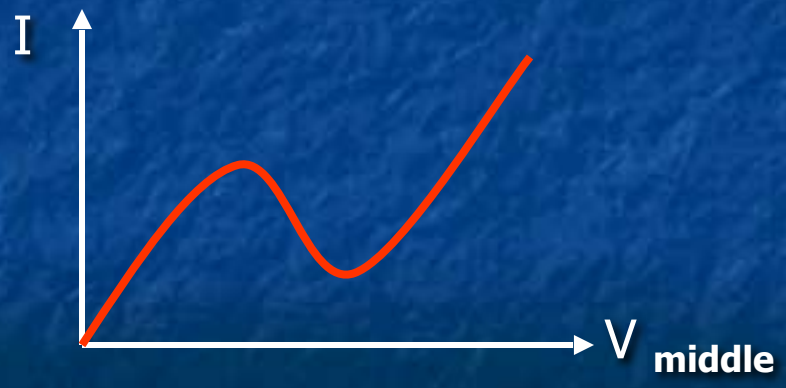
Negating the circuit simplification NDR's were supposed to offer? YES!

What if used paired NDR devices? And fixed the voltage across PAIR of NDR's:

What is going on with NDR $_1$?

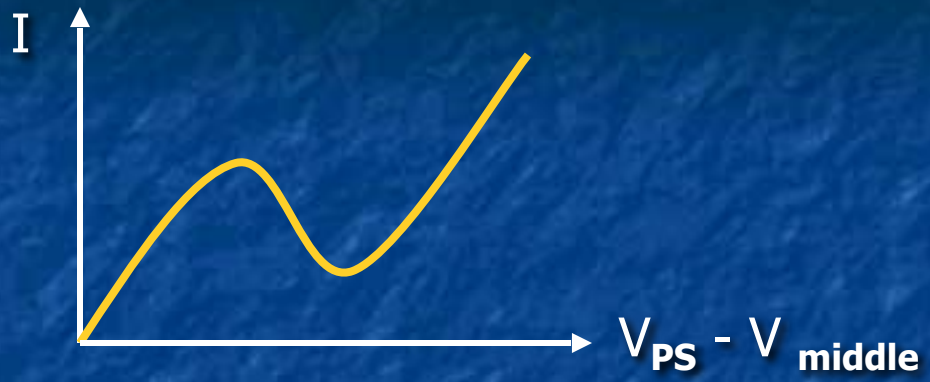
It's possible current flow vs. voltage:



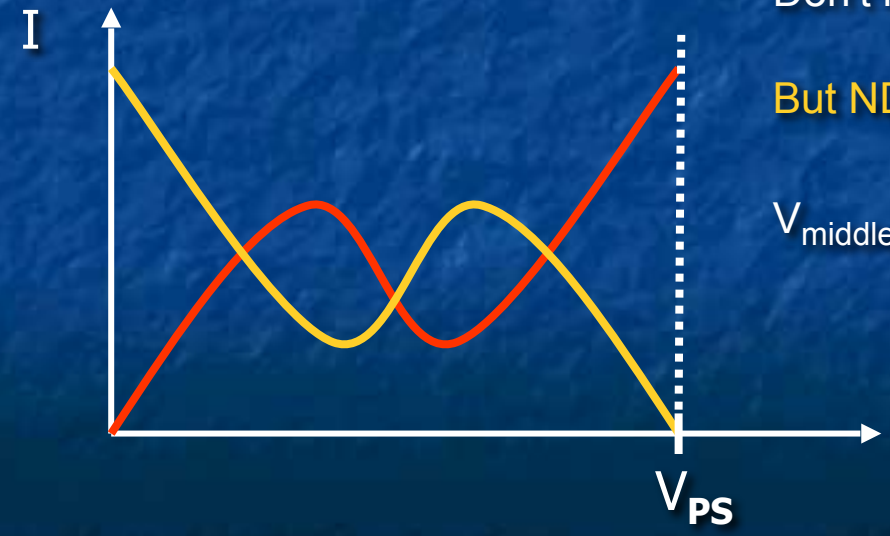


Leaving remainder of voltage for NDR_2

NDR $_2$:



NDR_2 gets leftover part of power supply voltage, so flip over onto first plot:

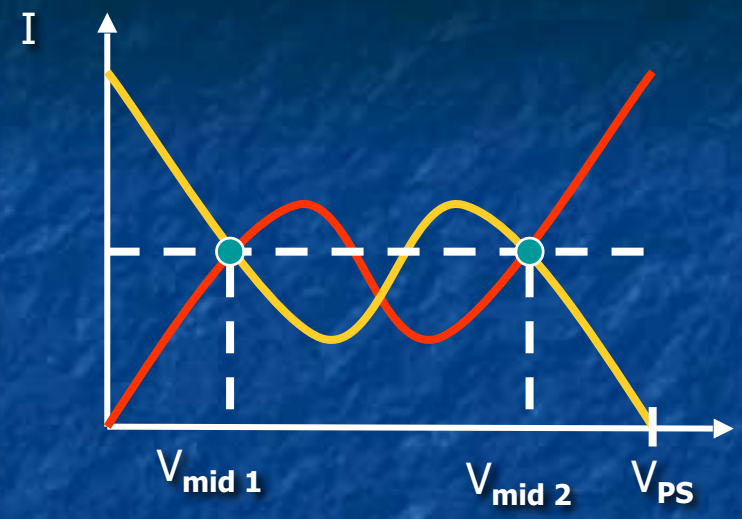


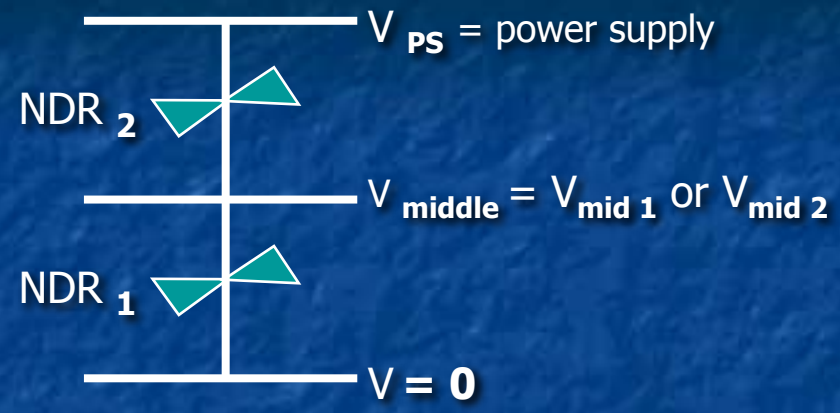
Don't initially know acceptable value of current, I

But NDRs are in series so MUST have SAME current

V_{middle} MUST settle to value where curves intersect →

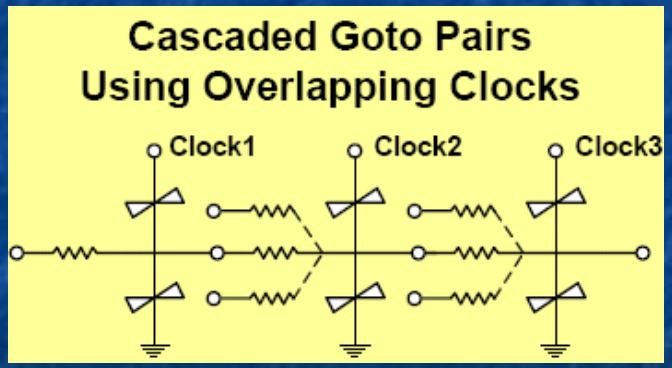
Center voltage of paired NDRs settles into one of two states

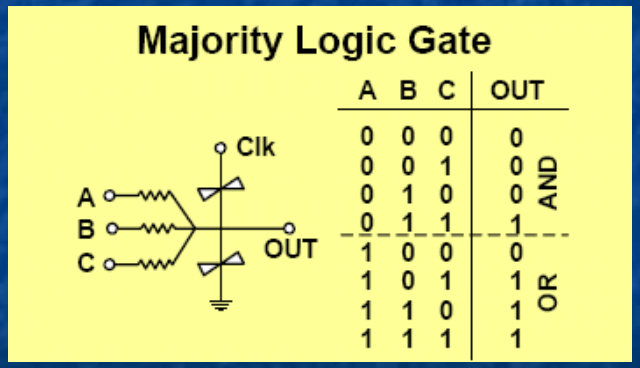




This strikingly simple but effective circuit = "Goto Pair" (after Japanese inventor)

Which combine into:





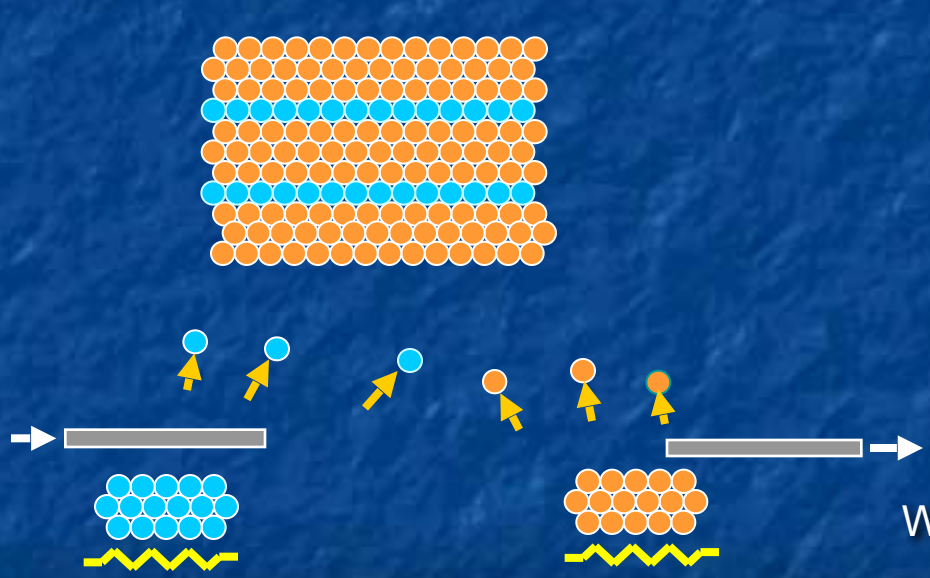
Design Approaches for Hybrid CMOS/Molecular Memory based on Experimental Device Data, G.S. Rose, A.C. Cabe, N. Gergel-Hackett, N. Majumdar, M.R. Stan, J.C. Bean, L.R. Harriott, Y. Yao, and J.M. Tour, Proc.16th ACM Great Lakes symposium on VLSI, pp. 2 - 7 (2006)

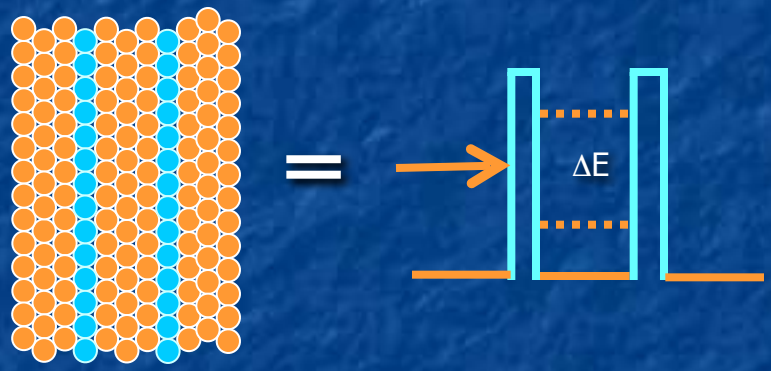
And there are LOTS of ways of creating required energy diagram!

One actually predates current nano craze:

Developed in 1980's when we already knew how to grow VERY THIN crystal layers

Used "Molecular Beam Epitaxy" (atomic spray painting – self-assembly lecture)

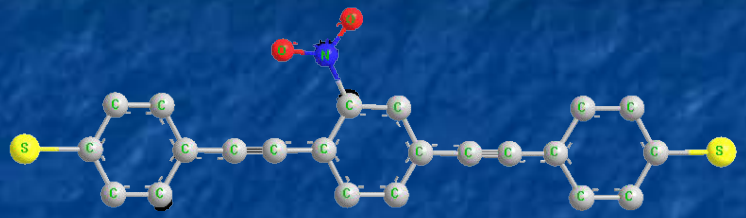




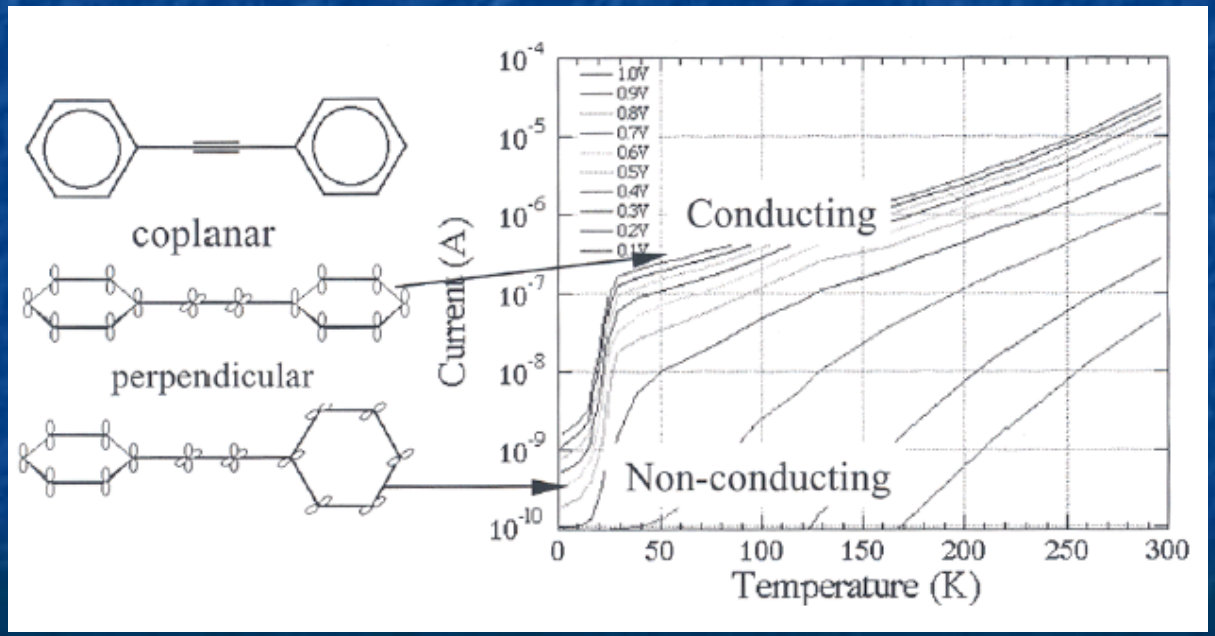
Were called “Resonant Tunneling Diodes" (RTDs)
In that incoming electron wave had
to resonate with bound level in center layer

An entirely different way of making an NDR (or NDR like) device:

That molecule I described in second slide of first lecture:



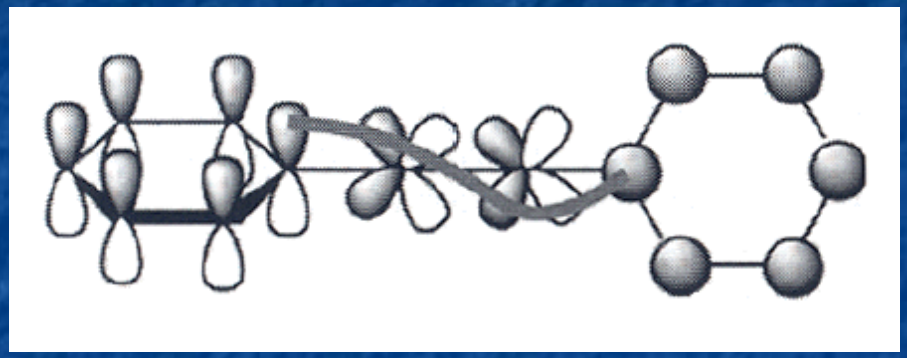
Current changes as such molecules twist under an applied voltage



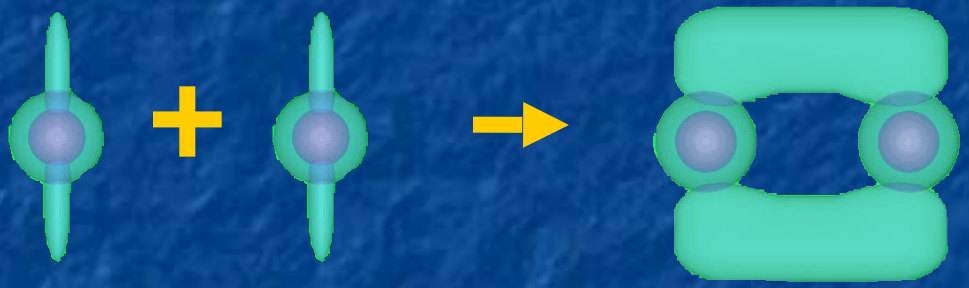
J. Chen and M.A. Reed, J. Chem. Phys 281, p127 (2002)

Still barriers & tunneling, but described in terms of Pi electron orbitals:

Pi electrons were the strange ones that stuck out perpendicular to main bonds



If have pi electrons on adjacent atoms, bridge together to form conductive pi bonds

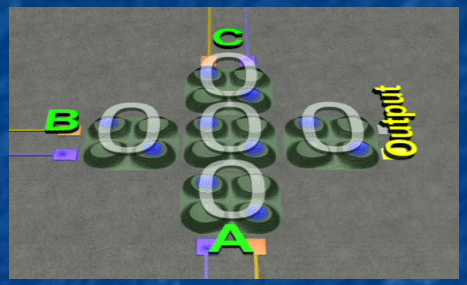


But as molecule twisted by voltage, alignment is lost, pi bonds weaken → NDR

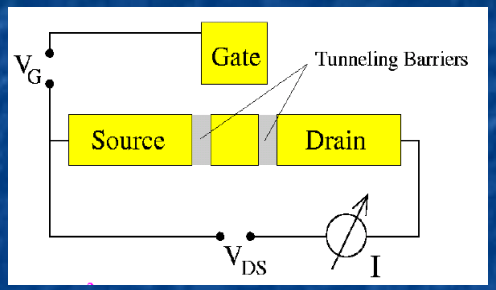
(or at least, that is ONE of the theories!)

Giving at least three very weird ways of getting digital devices:

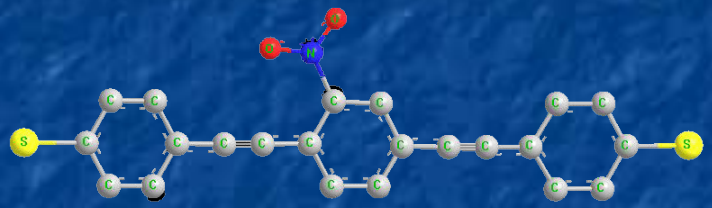
QCA's:



SETs':



NDR's:



Which MIGHT emulate/surpass transistor digital circuits

But by making use of VERY WEIRD non-transistor devices

DISCLAIMER: None of these **particular** schemes has yet succeeded (and may never!)

But they are **true** nanoelectronic alternatives (along with many, many others)

And show that nanoelectronics will probably NOT be shrunken version of microelectronics!

Credits / Acknowledgements

Funding for this class was obtained from the National Science Foundation (under their Nanoscience Undergraduate Education program).

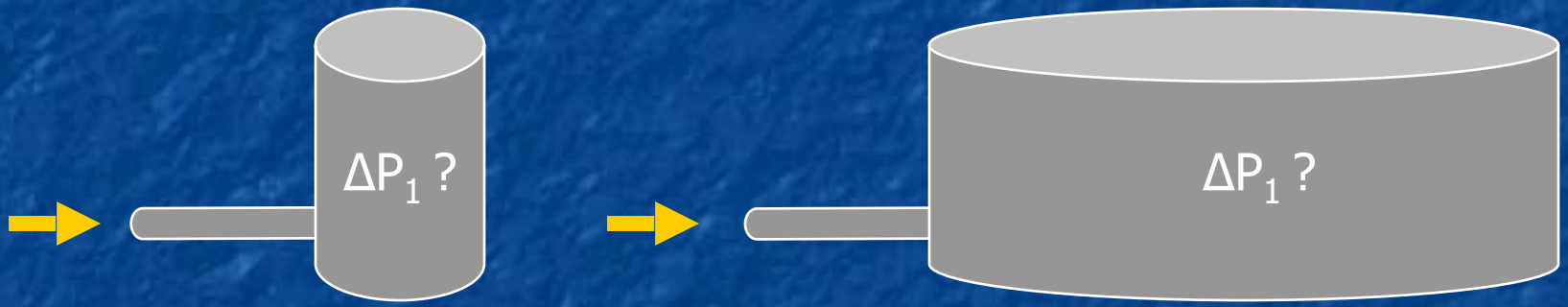
This set of notes was authored by John C. Bean who also created all figures not explicitly credited above.

NOTE:
Special appendix quantifying Coulomb Blockade nanoelectronic devices follows this slide

Appendix Quantifying Coulomb Blockade behavior:

Need to expand understanding of "capacitors." Use gas storage analogy:

Move a fixed amount of air into tanks of different size:



Will pressure changes be the same? Of course not:

MUCH more room for added air to spread out in bigger tank!

Pressure induced by addition of quantity of air is inversely proportional to volume:

That's what the ideal gas law states: PV = nRT or . . .

P α Quantity / Vol or using Q for quantity: P(Q) α Q / Vol

Work done to reach a given pressure?

NOT just proportional to amount of air added:

Because as air was added, had to fight increased pressure to add more!

So increment of work to add unit of air increases with pressure:

W (P) α P(Q) or from preceding page W (Q) α Q / Vol

= Work to add MORE air when have Q in tank increases as value of Q

So integrated energy expended in adding total quantity of air Q to tank is

$$\Delta E_{stored} \alpha Q^2 / 2 Vol$$

Recapping: $P \sim Q / Vol$ and $E \sim Q^2 / 2Vol$

Back to electrical world:

VOLTAGE corresponds PRESSURE CAPACITANCE corresponds to tank VOLUME

Capacitance is measure of a device structure's ability to store charge

Integrated circuits use "planar" technology ~ single layer of more or less flat devices

In such flat devices, capacitance varies as their surface area: $C = A (\varepsilon/d)$

Putting this all together for modern planar electronic devices, expect:

$P \sim Q_{gas}$ / Volume => Voltage = Q_{charge} / Capacitance

$E \sim Q_{gas}^2$ / 2 Volume => $E = Q_{charge}^2$ / 2 Capacitance

Using Q for quantity of air stored / quantity of charge stored

Use in quantifying effect of "coulomb blockades" ?

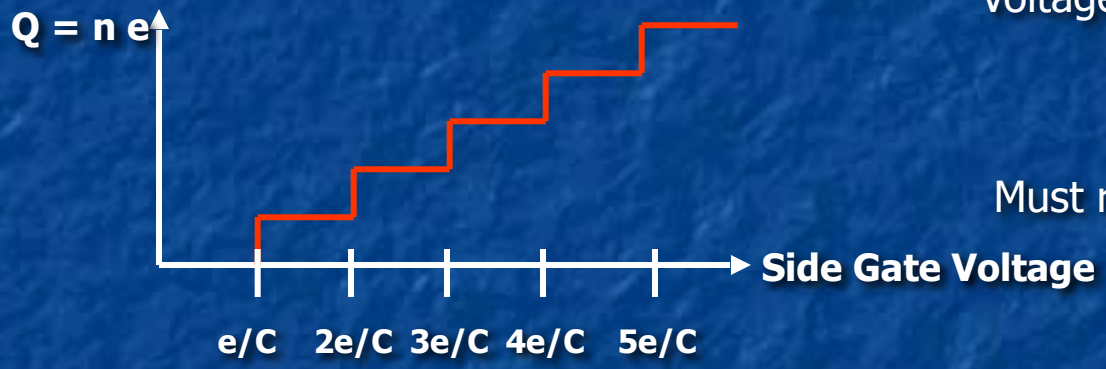
General formulas for capacitors were:

Charge stored: $Q = C V$ Voltage: $V = Q/C$ Energy stored: $E = Q^2 / 2 C$

On nano capacitor (Q-dot + side gate) # of charges stored = n. Each with electron charge e:

Charge stored: $Q = ne = CV$ Voltage: $V = ne/C$ Energy stored: $E = n^2 e^2 / 2 C$

Yielding this strange charge vs. voltage plot:



Voltage jumps each time one electron added

OR

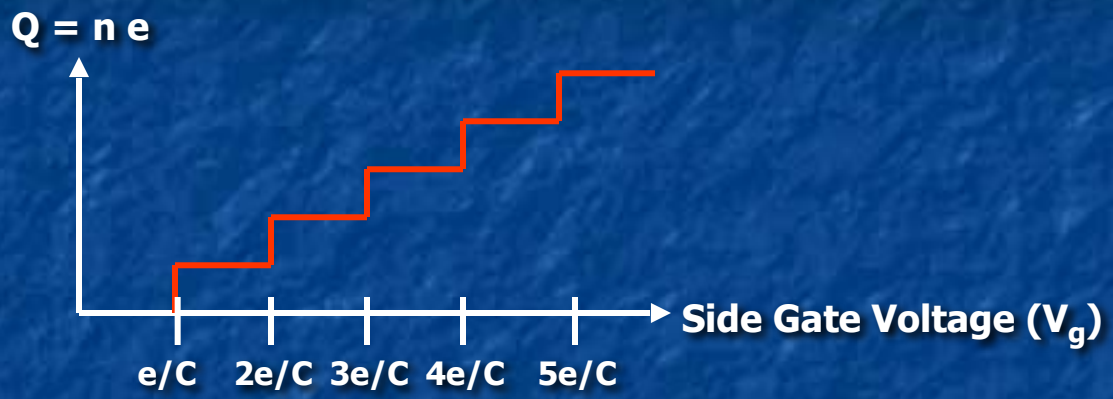
Must raise voltage e/C to add new electron

BIG capacitor: Steps so close together => continuous upward sloping line

NANO capacitor: Steps far apart and VERY significant => "Blockade"

Translating this into device "conductance" = dI_{ds} / dV_g:

Q vs. side gate voltage plot:



Translates into conductance plot of: